PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:	**Thomas J. Sullivan**		
Serial No.:	09/491,810	Art Unit:	2183
Filed:	January 28, 2000	Examiner:	Meonske, Tonia L.
For:	AN APPARATUS AND METHOD FOR PERFORMING SINGLE-INSTRUCTION MULTIPLE DATA INSTRUCTIONS	Docket No.:	10981801-1

RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

Mailstop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In regard to the outstanding Notice of Non-Compliant Appeal Brief of December 29, 2005, Applicants submit the following remarks.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. §1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company, L.P. Deposit Account No. 08-2025.

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope, with sufficient postage, addressed to: Mailstop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA, 22313-1450 on 1-9-06.

Signature: Shana K. East

REMARKS

In the outstanding Notice of Non-Compliant Appeal Brief of December 29, 2005, it is asserted that Applicants' replacement section for the summary of claimed subject matter filed on October 17, 2005, is defective for allegedly failing to contain a concise explanation of the subject matter defined in independent claim 16. A summary of the claimed subject matter for independent claims 16 and 26 is set forth below pursuant to M.P.E.P. §1205.03(B). Applicants respectfully assert that the below summary corrects for the alleged defects described by the Notice of Non-Compliant Appeal Brief.

Summary of Claimed Subject Matter

The summary is set forth as exemplary embodiments of claims 16 and 26. Discussions about elements and recitations can be found at least at the cited locations in the specification and drawings.

As embodied in claim 16, an apparatus is provided for performing single-instruction multiple data (SIMD) operations using one multiply-accumulate (MAC) unit. (e.g., paragraph 0005). In this regard, a MAC unit (e.g., reference numeral 41) is coupled to operand buses (e.g., reference numerals 22, 23, and 24) at respective operand inputs (e.g., paragraph 0015, lines 1-8). The MAC unit is configured to latch a first multiple-bit data value during a first cycle and execute the MAC functions on the first multiple-bit data vale during the next subsequent cycle while latching a second multiple-bit data value (e.g., paragraph 0026, lines 2-6, and paragraph 0027, lines 1-3). The MAC unit is further configured to supply a first MAC result responsive to the first multiple-bit data value on a result bus (e.g., reference numeral 47 once the first MAC result is

available (e.g., paragraph 30, lines 1-3) and latch a second MAC result responsive to the second multiple-bit data value (e.g., paragraph 0033, lines 1-3). A register (e.g., reference numeral 80) is coupled to the result bus and is configured to latch the first MAC result (e.g., Paragraph 0018, lines 7-12). A miscellaneous logic unit (e.g., reference numeral 32) is coupled between the result bus and the register (e.g., Figure 2), and the miscellaneous logic unit is configured to detect one or more exceptional conditions (e.g., paragraph 0031, lines 1-2, and paragraph 0033, lines 1-3). The miscellaneous logic unit is further configured to generate first and second control signals responsive to at least one certain exceptional condition, wherein when the first control signal is asserted the MAC unit supplies the second MAC result on the result bus (e.g., paragraph 0031, lines 1-8, and paragraph 0033, lines 1-2). When the second control signal is asserted, the first MAC result is driven from the register onto the result bus (e.g., paragraph 0033, lines 3-5). When the second control signal is not asserted, a miscellaneous-unit generated result is driven onto the result bus (e.g., paragraph 0031, lines 1-2, and paragraph 0034, lines 1-3).

As embodied in claim 26, an apparatus is provided. In this regard, a means (e.g., reference numeral 31) for producing control signals is responsive to a first data value, a second data value, and one or more exceptional conditions (e.g., paragraph 27, lines 3-4; paragraph 31, lines 1-4; and Fig. 2). The exceptional conditions result from the execution of a multiply accumulate (MAC) unit (e.g., reference numeral 41) over the first and second data values in sequential order, and the means for producing is configured to detect the one or more exceptional conditions (e.g., paragraph 33, lines 1-5; paragraph 34, lines 1-3; and Fig. 2). A means (e.g., reference numerals 80, 51A, 51B, 61A, 61B, 71A, 28) for arranging a combination selected from a first MAC unit result, a second MAC unit result, and a representation of a specific exceptional condition is responsive to the

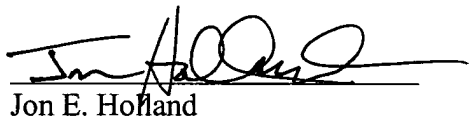
plurality of control signals, and the control signals direct whether the first MAC unit result and the second MAC unit result should be used or replaced by the representation of the specific exceptional condition, respectively (e.g., paragraph 31, lines 1-8; paragraph 32; paragraph 33, lines 1-5; paragraph 34, lines 1-3; paragraph 35, lines 1-4; paragraph 39, lines 2-4; and Fig. 2).

CONCLUSION

Applicants respectfully request that the Patent Office accept and consider the Appeal Brief filed on July 19, 2005. If the Examiner has any questions or comments regarding this paper, the Examiner is encouraged to telephone Applicants' undersigned counsel.

Respectfully submitted,

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.

By: 

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